§112 Rejection of the Claims

Claims 1-45 were rejected under 35 USC § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. The rejection states:

> Claims 1-5, 10-12, 17, 23, 25, 29, 32, 33, 37-40, 44, and 45 are misdescriptive and renders the claims indefinite as reciting the pair of transistors M3, M5 and M4, M6 is a dual-gated transistor. It is well known in the art that a dual gated transistor is an AND function circuit.

In the art there are dual gated transistor having two gates only on one side of a transistor, e.g. Cuevas, and there are dual gated transistors having each gate on opposite sides of the transistor. Applicant has invited the Examiner to confirm the same in reference to US patent number 6,104,068 which further supports the Applicant's lexicography. Applicant respectfully renew its request that reference to this illustrative patent be addressed as evidencing that dual gated transistors have been described, by the present inventor, which perform the OR function. All dual-gated transistors do not perform the AND function. And, all dual-gated transistors do not function as "two transistors connected in series," as recited in paragraph 9 of the present office action. Certainly the one shown in Cuevas does, but this is not the entire universe of dual gate transistor types. Applicant's reference to US patent number 6,104,068 evidences the fact that some dual-gated transistors act as "two transistors connected in parallel, performing the OR function. Acknowledgment of the same in view of patent 6,104,068 is respectfully requested. Accordingly, reconsideration and withdrawal of the 112 rejection of the above claims in respectfully requested in view of patent 6,104,068.

§102 Rejection of the Claims

Claims 1-7, 10-14, 17-20, 29, 32-39, 44 and 45 were rejected under 35 USC § 102(b) as being anticipated by Kawashima (U.S. 5699,305). The rejection states:

> Kawashima discloses in figure 7 a sense amplifier (105) comprising: a pair of cross-coupled inverters (66-69, and 72-75), wherein each inverter includes: a transistor of a first conductivity type (66, 67), a dual gated transistor of second conductivity type (68, 69, 74, 75) wherein a drain region for the dual-gated transistor is coupled to a drain region of the transistor of the first conductivity type; a pair of bit lines (IN, /IN), wherein each one of the pair of bit lines is coupled to a first gate of the dual-gated transistor in each inverter; and a pari of bit lines is coupled to a first gate of the dual-gated transistor in each inverter; and a pair of output transmission lines (OUT, /OUT), wherein each one of the pair of output transmission lines is coupled to the drain region of the dual-gated transistor and the drain region of the transistor of the first conductivity type in each inverter.

Kawashima appears to describe an amplifier and semiconductor memory device having the same. The amplifier is coupled to first and second power supply lines. Kawashima further describes a first pair of cross-coupled transistors connected to the first power supply line and a pair of output terminal, and a second pair of cross-coupled transistors connected to the second power supply line. Kawashima does not describe or teach a pair of cross-coupled inverters/amplifier, each inverter having a dual-gate transistor, or pair of transistors of a second conductivity type wherein a drain region for the dual-gate transistor in each inverter is coupled to a drain region of the transistor of the first conductivity type in the same inverter, and coupled directly to a gate of the transistor of the first conductivity type in the other inverter of the pair of cross-couple inverters, and coupled to one gate of the dual-gate transistor in the other inverter of the pair of cross-couple inverters.

In an effort to advance the prosecution of the present case, Applicant has amended each independent claim in the pending claimset. These amendments are fully supported by the Applicant's specification on page 9 line 24 through page 10 line 3. The amendments in part reapply language which was removed from the claims in response to the first office action. These independent claims, as amended, recite a pair of cross-coupled inverters/amplifier, each

inverter having "a dual-gate transistor, or pair of transistors, of a second conductivity type wherein a drain region for the dual-gate transistor in each inverter is coupled to a drain region of the transistor of the first conductivity type in the same inverter, coupled **directly** to a gate of the transistor of the first conductivity type in the other inverter of the pair of cross-couple inverters, and coupled to one gate of the dual-gate transistor, or pair of transistors, in the other inverter of the pair of cross-couple inverters."

Since the Kawashima reference neither describes or suggest such a configuration, Applicant respectfully submits that the reference can no longer support the 102 rejection for the above claims. Accordingly, reconsideration and withdrawal of the 102 rejection is respectfully requested.

§103 Rejection of the Claims

Claims 8, 9, 15-22 and 30-31 were rejected under 35 USC § 103(a) as being unpatentable over Kawashima (U.S. 5,699,305). Each of these claims either depends from or includes an amended independent claim as described above. For the same reasons presented above, the independent claims are believed to clearly distinguish from the Kawashima reference. Accordingly, reconsideration and withdrawal of the 103 rejection for these claims is respectfully requested.

Claims 23-28 and 40-43 were rejected under 35 USC § 103(a) as being unpatentable over Kaneko et al (U.S. 6,069,828) in view of Kawashima (U.S. 5699,305). The Kaneko reference does not cure the deficiencies of the Kawashima reference for the above amended independent claims. For the arguments presented above, the Applicant believes that each of the pending independent claims, as amended, is allowable over Kawashima. Since each and every element of the Applicant's independent claims, as amended, is neither described or suggested by the references, either independently or in combination, reconsideration and withdrawal of the 103 rejection for the above claims is requested.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney (612- 373-6913) to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

LEONARD FORBES ET AL.

By their Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938
Minneapolis, MN 55402
(612) 373-6913

Date 4/12/2001 By _____
Edward J. Brooks, III
Reg. No. 40,925

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Box AF, Commissioner of Patents, Washington, D.C. 20231, on this 12th day of April, 2001.

Amy Moriarty
Name

_____
Signature

Docket No. 303.586US1 Micron Ref. No. 98-0588
WD # 320804

Clean Version of Pending Claims

DRAM SENSE AMPLIFIER FOR LOW VOLTAGES
Applicant: Leonard Forbes et al.
Serial No.: 09/320,421

Claims 1-2, 4, 6-11, 13-18, 20-24, 26-38 and 40-45, as of April 12, 2001 (response to final office action filed).

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1. (Twice Amended) A sense amplifier, comprising:

a pair of cross-coupled inverters, wherein each inverter includes:

a transistor of a first conductivity type;

a pair of transistors of a second conductivity type coupled at a drain region and coupled at a source region, and wherein the drain region for the pair of transistors in each inverter is coupled to a drain region of the transistor of the first conductivity type in the same inverter, is coupled directly to a gate of the transistor of the first conductivity type in the other inverter of the pair of cross-couple inverters, and is coupled to a gate of one of the pair of transistors in the other inverter of the pair of cross-couple inverters;

a pair of input transmission lines, wherein each one of the pair of input transmission lines is coupled to a gate of one of the pair of transistors in each inverter; and

a pair of output transmission lines, wherein each one of the pair of output transmission lines is coupled to the drain region of the pair of transistors and the drain region of the transistor of the first conductivity type in each inverter.

2. (Twice Amended) The sense amplifier of claim 1, wherein the transistor of a first conductivity type is a p-channel metal oxide semiconductor (PMOS) transistor, and wherein the pair of transistors of a second conductivity type are n-channel metal oxide semiconductor (NMOS) transistors.

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4. (Twice Amended) A sense amplifier, comprising:

a pair of cross-coupled inverters, wherein each inverter includes:

a p-channel metal oxide semiconductor (PMOS) transistor; and

a pair of n-channel metal oxide semiconductor (NMOS) transistors coupled at a drain region and a source region, and wherein a drain region of the PMOS transistor in each inverter is coupled to the drain region for the pair of NMOS transistors in the same inverter, is coupled directly to a gate of the PMOS transistor in the other inverter of the pair of cross-couple inverters, and is coupled to a gate of one of the pair of NMOS transistors in the other inverter of the pair of cross-couple inverters;

a bit line coupled to each inverter, wherein each bit line couples to a gate of one of the pair of NMOS transistors in each inverter; and

a pair of output transmission lines, wherein each one of the pair of output transmission lines is coupled to the drain region for the PMOS and the NMOS transistors in each inverter respectively.

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6. The sense amplifier of claim 4, wherein the bit line capacitances are removed from the pair of output transmission lines.

7. The sense amplifier of claim 6, wherein each bit line is coupled to a number of memory cells in an array of memory cells.

8. The sense amplifier of claim 4, wherein the sense amplifier is coupled to a power supply voltage of less than 1.0 Volts.

9. The sense amplifier of claim 8, wherein the sense amplifier is able to output a full output sense voltage in less than 10 nanoseconds (ns).

10. (Twice Amended) A latch circuit, comprising:

a pair of cross-coupled amplifiers, wherein each amplifier includes:

a first transistor of a first conductivity type;

a second transistor and a third transistor of a second conductivity type, wherein the second and the third transistor in each amplifier are coupled at a drain region and are coupled at a source region, and wherein a drain region for the second and the third transistors are coupled to a drain region of the first transistor in the same amplifier, are coupled directly to a gate of the first transistor of the first conductivity type in the other amplifier in the pair of cross-coupled amplifiers, and are coupled to a gate of the third transistor in the other amplifier in the pair of cross-coupled amplifiers;

a pair of input transmission lines, wherein each one of the pair of input transmission lines is coupled to a gate of the second transistor in each amplifier; and

a pair of output transmission lines, wherein each one of the pair of output transmission lines is coupled to the drain region of the first transistor and to the drain region of the second and the third transistors.

11. (Twice Amended) The latch circuit of claim 10, wherein the first transistor includes a p-channel metal oxide semiconductor (PMOS) transistor, and wherein the second and the third ransistors include n-channel metal oxide semiconductor (NMOS) transistors.

13. The latch circuit of claim 10, wherein the pair of input transmission lines are bit lines and wherein the bit line capacitances are removed from the pair of output transmission lines.

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14. The latch circuit of claim 13, wherein each bit line is coupled to a number of memory cells in an array of memory cells.

15. The latch circuit of claim 10, wherein the latch circuit is coupled to a power supply voltage of less than 1.0 Volts.

16. The latch circuit of claim 10, wherein the latch circuit is able to output a full output sense voltage in less than 10 nanoseconds (ns).

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17. (Once Amended) An amplifier circuit, comprising:

a pair of cross-coupled inverters, wherein each inverter includes:

a transistor of a first conductivity type;

a dual-gated metal-oxide semiconducting field effect transistor (MOSFET) of a second conductivity type, wherein the transistor of a first conductivity type in each inverter and the a dual-gated MOSFET are coupled at a drain region in the same inverter, and wherein the drain region in each inverter is further coupled directly to a gate of the transistor of the first conductivity type in the other inverter of the pair of cross-couple inverters, and is coupled to one gate of the dual-gated MOSFET in the other inverter of the pair of cross-couple inverters;

a pair of input transmission lines, wherein each one of the pair of input transmission lines is coupled to another gate of the dual-gated MOSFET in each inverter respectively; and

a pair of output transmission lines, wherein each one of the pair of output transmission lines is coupled to the drain region on each one of the pair of cross-coupled inverters.

18. The amplifier circuit of claim 17, wherein the transistor of a first conductivity type includes a p-channel metal oxide semiconductor (PMOS) transistor, and wherein the dual-gated MOSFET of a second conductivity type is divided into two separate n-channel metal oxide semiconductor (NMOS) transistors each driven by one of the dual gates.

20. The amplifier circuit of claim 17, wherein the pair of cross-coupled inverters comprise a sense amplifier, and wherein the sense amplifier is included in a memory circuit.

21. The amplifier circuit of claim 20, wherein the sense amplifier is coupled to a power supply voltage of less than 1.0 Volts.

22. The amplifier circuit of claim 21, wherein the sense amplifier is able to output a full output sense voltage in less than 10 nanoseconds (ns).

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23. (Twice Amended) A memory circuit, comprising:
a number of memory arrays;
at lease one sense amplifier, wherein the sense amplifier includes:
a pair of cross-coupled inverters, wherein each inverter includes:
a p-channel metal oxide semiconductor (PMOS) transistor; and
a dual-gate metal oxide semiconductor (NMOS) transistor
wherein a drain region of the PMOS transistor in each inverter is coupled to a drain region of for the dual-gate NMOS transistor in the same inverter, is coupled directly to a gate of the PMOS transistor in the other inverter of the pair of cross-couple inverters, and to one gate of the dual-gate NMOS

transistor in the other inverter of the pair of cross-couple inverters;

a complementary pair of bit lines coupling the at least one sense amplifier to a number of memory cells in the number of memory arrays, and wherein each one of the complementary pair of bit lines couples to a gate of the dual-gate NMOS transistor in each inverter; and

a pair of output transmission lines, wherein each one of the pair of output transmission lines is coupled to the drain region of the PMOS transistor and the drain region for the dual-gate NMOS transistor in each inverter.

24. The memory circuit of claim 23, wherein the memory circuit includes a folded bit line memory circuit.

26. The memory circuit of claim 23, wherein the at least one sense amplifier is coupled to a power supply voltage of less than 1.0 Volts.

27. The memory circuit of claim 23, wherein the at least one sense amplifier is able to output a full output sense voltage in less than 10 nanoseconds (ns).

28. The memory circuit of claim 23, wherein the memory circuit further includes a number of equilibration and a number of isolation transistors coupled to the complementary pair of bit lines.

29. (Twice Amended) An electronic system, comprising:

a processor;

a memory device; and

a bus coupling the processor and the memory device, the memory device further including a sense amplifier, comprising:

a pair of cross-coupled inverters, wherein each inverter includes:

a p-channel metal oxide semiconductor (PMOS) transistor; and

a dual-gate metal oxide semiconductor (NMOS) transistor wherein a drain region of the PMOS transistor in each inverter is coupled to a drain region for the dual-gate NMOS transistor in the same inverter, is coupled directly to a gate of the PMOS transistor in the other inverter of the pair of cross-couple inverters, and is coupled to one gate of the dual-gate NMOS transistor in the other inverter of the pair of cross-couple inverters;

a complementary pair of bit lines coupling the at least one sense amplifier to a number of memory cells in a memory cell array, and wherein each one of the complementary pair of bit lines couples to a gate of the dual-gate NMOS transistor in each inverter; and

a pair of output transmission lines, wherein each one of the pair of output transmission lines is coupled to the drain region of the PMOS transistor and the drain region for the dual-gate NMOS transistor in each inverter.

30. The electronic system of claim 29, wherein the sense amplifier is coupled to a power supply voltage of less than 1.0 Volt.

31. The electronic system of claim 29, wherein the sense amplifier is able to output a full output sense voltage in less than 10 nanoseconds (ns).

32. (Twice Amended) An integrated circuit, comprising:

a processor;

a memory operatively coupled to the processor; and

wherein the processor and memory are formed on the same semiconductor substrate and the integrated circuit includes at least one sense amplifier, comprising:

a pair of cross-coupled inverters, wherein each inverter includes:

a transistor of a first conductivity type;

a dual-gate transistor of a second conductivity type wherein a drain region for the dual-gate transistor in each inverter is coupled to a drain region of the transistor of the first conductivity type in the same inverter, is coupled directly to a gate of the transistor of the first conductivity type in the other inverter of the pair of cross-couple inverters, and to one gate of the dual-gate transistor in the other inverter of the pair of cross-couple inverters;

a pair of bit lines, wherein each one of the pair of bit lines is coupled to a [first] gate of the dual-gate transistors in each inverter; and

a pair of output transmission lines, wherein each one of the pair of output transmission lines is coupled to the drain region of the dual-gate transistor and the drain region of the transistor of the first conductivity type in each inverter.

33. (Twice Amended) A method for forming a current sense amplifier, comprising:

cross coupling a pair of inverters, wherein each inverter includes:

a transistor of a first conductivity type;

a dual-gate transistor of a second conductivity type wherein a drain region for the dual-gate transistor is coupled to a drain region of the transistor of the first conductivity type; and

wherein cross coupling the pair of inverters includes directly coupling the drain region for the transistor of the first conductivity type and the drain region for the dual-gate transistor in one inverter to a gate of the transistor of a first conductivity type and to one gate of the dual-gate transistor in the other inverter.

34. The method of claim 33, wherein cross coupling the pair of inverters includes forming the first transistor of the first conductivity type as a p-channel metal oxide semiconductor (PMOS) transistor, and forming the dual-gate transistor of a second conductivity type as an n-channel metal oxide semiconductor (NMOS) transistor.

35. (Twice Amended) The method of claim 33, wherein the method further includes coupling a bit line to another gate of the dual-gate transistor in each inverter.

36. The method of claim 33, wherein the method further includes coupling an output transmission line to the drain region for the dual-gate transistor and the drain region of the transistor of the first conductivity type in each inverter. .

37. (Twice Amended) A method for forming a sense amplifier, comprising:

forming and cross coupling a pair of inverters, wherein forming and cross coupling each inverter includes:

forming a first transistor of a first conductivity type;

forming a dual-gate transistor of a second conductivity type, wherein forming the dual-gate transistor includes coupling the drain region for the dual-gate transistor to a drain region of the first transistor in each inverter, directly coupling the drain region for the dual-gate transistor in each inverter to a gate of the first transistor of the first conductivity type in the other inverter and to a gate of the dual-gate transistor of the second conductivity type in

the other inverter;

coupling a bit line to a gate of the dual-gate transistor in each inverter; and

coupling an output transmission line to the drain region of the first transistor and to the drain region of the dual-gate transistor in each inverter.

38. The method of claim 37, wherein forming the first transistor of a first conductivity type includes forming a p-channel metal oxide semiconductor (PMOS) transistor, and wherein forming the dual-gate transistor of a second conductivity type includes forming an n-channel metal oxide semiconductor (NMOS) transistor.

40. (Twice Amended) A method for operating a sense amplifier, comprising:

equilibrating a first and second bit line, wherein the first bit line is coupled to a first gate of a dual-gate transistor in a first inverter in the sense amplifier and the second bit lines is coupled to a first gate of a dual-gate transistor in a second inverter in the sense amplifier;

discharging a memory cell onto the first bit line, wherein discharging a memory cell onto the first bit line drives a signal from a drain region for the first inverter directly to a gate of a PMOS transistor and to a second gate of a dual-gate transistor in the second inverter; and

providing a feedback from a drain region for the second inverter to a gate of a PMOS transistor and a second gate of a dual-gate transistor in the first inverter.

41. The method of claim 40, wherein operating the sense amplifier includes operating the sense amplifier with a power supply voltage of less that 1.0 Volts.

42. The method of claim 40, wherein operating the sense amplifier includes latching an output sense signal in less than 10 nanoseconds (ns).

43. The method of claim 40, wherein the method further includes removing the bit line capacitance from a pair of output nodes of the sense amplifier.

44. (Twice Amended) A method for operating a sense amplifier, comprising:

providing a first bit line signal to a first gate of a dual-gate transistor in a first inverter of the sense amplifier;

providing a second bit line signal to a first gate of a dual-gate transistor in a second inverter of the sense amplifier

wherein providing the first and the second bit line signals to the first gates of the dual-gate transistors drives a signal directly from a drain region for the first inverter to a gate of a PMOS transistor and to a second gate of a dual-gate transistor in the second inverter; and

wherein providing the first and the second bit line signals to the first gates of the dual-gate transistors isolates the bit line capacitances from a first and second output node on the sense amplifier.

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45. (Twice Amended) A method for operating a sense amplifier, comprising:

providing an input signal from a bit line to a first gate of a dual-gate transistor in a first inverter of the sense amplifier

wherein providing the input signal from the bit line to the first gate of the dual-gate transistor in the first inverter of the sense amplifier drives a signal directly from a drain region for the first inverter to a gate of a PMOS transistor and to a gate of a dual-gate transistor in a second inverter; and

wherein providing the input signal to the first gate of the dual-gate transistor isolates the bit line capacitance from an output node on the sense amplifier.